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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,121	06/19/2003	Zheng John Shen	104023-361-NP	6010

7590 11/22/2004

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EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,121	SHEN, ZHENG JOHN	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "second conductivity" and "first conductivity" in lines 1 and 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "second conductivity" and "first conductivity" in lines 1 and 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-15, 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Efland et al.

Regarding claim 1, Efland et al discloses on figure 2G a semiconductor device comprising a semiconductor substrate 54; at least on first doped region 58 in said semiconductor substrate forming at least one source; at least one second doped region 64 in said semiconductor substrate forming at least one drain; a first connectivity layer 21a having at least one first runner 21a (on the left hand side) and at least one second runner 21a(on the right hand side), wherein said at least one first runner is operatively connected to said at least one first doped region 58 and said at least one second runner is operatively connected to said at least one second doped region 64; a second connectivity layer 21b connected to said first connectivity layer and having at least one third runner 21b (on the right hand side) and at least fourth runner (on the left hand side), wherein said at least one third runner is operatively connected to said at least one first runner and said at least one fourth runner is operatively connected to said at least one second runner; a third connectivity having at least one first pad 38 (on the right hand side) connected to said at least one third runner and at least one second pad 38 (on the left hand side) operatively connected to said at least one fourth runner.

Regarding claim 2, Efland et al discloses on figure 2G said at least one first pad has at least one first solder bump 38 (on the right hand side) and said at least second pad has at least one second solder bump (on the left hand side).

Regarding claim 3, Efland et al discloses on figure 1B said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

Regarding claim 4, Efland et al discloses on figure 2G said at least one first pad is interleaved with said at least one second pad.

Regarding claim 5, Efland et al discloses on figure 2G said at least one first doped region 58 is a source for a transistor and said at least one second region 64 is a drain for a transistor.

Regarding claim 6, Efland et al discloses on figure 2G said at least one source 54 and at least one drain are laid out in a substantially elongated shape and wherein said at least one source is interleaved with said at least one drain.

Regarding claim 8, Efland et al discloses on figure 2G a semiconductor device comprising a semiconductor substrate 54; at least one first doped region 58 in said semiconductor substrate forming at least one source; at least one second doped region 64 in said semiconductor substrate forming at least one drain; a first connectivity layer 21a operatively connected to said at least one first doped region; a second connectivity layer 21b operatively connected to said first connectivity layer and operatively connected to said at least one second doped region 64.

Regarding claim 9, Efland et al discloses on figure 2G said second connectivity layer 21b said second connectivity layer 21b is operatively connected to said at least second dope region 64 through said first connectivity layer.

Regarding claim 10, Efland et al discloses on figure 2G said second connectivity layer 21b is operatively connected to said at least one second doped region 64 through said first connectivity layer using a portion of said connectivity layer for such connection.

Regarding claim 11, Efland et al discloses on figure 2G a third conductivity layer with at least one first pad 38 (on the right hand side) and at least one second pad 38 of such layer (on the left hand side) wherein said at least one first pad is operatively

connected to said first connectivity layer 21a and said at least one second pad is operatively connected to said second connectivity layer 21b.

Regarding claim 12, Efland et al discloses on figure 2G said at least one first pad has at least one first solder bump 38 and said at least second pad has at least one second solder bump 38.

Regarding claim 13, Efland et al discloses on figure 1B said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

Regarding claim 14, Efland et al discloses on figure 2G said at least one first pad is interleaved with said at least one second pad.

Regarding claim 15, Efland et al discloses on figure 2G said at least one source 58 and at least one drain 64 are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

Regarding claim 17, Efland et al discloses on figure 2G a semiconductor device comprising a semiconductor substrate 54; at least one first doped region 58 in said semiconductor substrate forming at least one source; at least second doped region 64 in said semiconductor substrate forming at least one drain; a first connectivity layer having a first runner 21a (on the left hand side) operatively connected to said at least one first doped region 58 and at least one second runner 21a (on the right hand side) operatively connected to said at least one second doped region 64; a second connectivity layer having at least one first pad 38 (on the left hand side) operatively connected to said at least one first runner and at least second pad 38 (on the right hand side) operatively connected to said at least one second runner.

Regarding claim 18, Efland et al discloses on figure 2G said at least first pad has at least one first solder bump and said at least one second pad has one second solder bump.

Regarding claim 19, Efland et al discloses on figure 1B said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

Regarding claim 20, Efland et al discloses on figure 2G said at least one first pad is interleaved with said at least one second pad.

Regarding claim 21, Efland et al discloses on figure 2G said at least one source 58 and at least one drain 64 are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 16, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Efland et al as applied to claims 1, 8 and 18 above, and further in view of Eden et al.

Regarding claims 7, 16 and 22, Efland et al discloses on figure 2G substantially all the structure set forth in the claimed invention except said at least one source and at least one drain being laid out in a substantially checkerboard pattern. However, Eden et al disclose on figure 10 said at least one source and at least one drain being laid out in

a substantially checkerboard pattern. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Efland et at by having said at least one source and at least one drain being laid out in a substantially checkerboard pattern for the purpose of reducing the inductance and resistance of the electrical connection as taught by Eden at al (col. 13, lines 62-63).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

JN
November 16, 2004.

JEROME JACKSON
PRIMARY EXAMINER